GENERIC INTERCONNECTION BUS SYSTEM FOR CHIPS WITH FPGA TECHNOLOGY

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ABSTRACT

This paper deals with design of interconnection bus system for chips with FPGA technology. The system ensures both communication between internal components on a chip and their communication with other computer devices which are mapped to the host system memory. The buses are high-speed, full duplex and packet-oriented and their architecture is based on tree topology. The data width is configurable, individually for every bus part. Due to this feature, it is possible to build uniform hierarchical system of internal buses with different speed that interconnects differently fast components. Interconnection system is being developed under the Liberouter project which is the part of CESNET research intention Programmable Hardware [1].

1. INTRODUCTION

Computing systems at any level are getting more and more complex. It is essential to design such systems enough modularly and universally to be well scalable and easily maintainable. Individual modules have to communicate with each other to be able to exchange data in a defined way. They have to be mutually interconnected.

This is also important for systems based on FPGA technology. Firstly, the communication capability between internal components on a chip needs to be provided. In case that FPGA gate array is the part of device connected to PC, also the communication with processor and other computer elements has to be supported.

Significant part of each application implemented on FPGA chip is interconnection bus system. Considering that the bus throughput is often limiting factor of designed solutions, it is necessary for such a system to be enough effective. On the other hand, it is also desirable to be compact and does not occupy too much chip area so that it does not limit implemented application. There are many other requirements that can be put on FPGA interconnection systems and their satisfying is closely related to the choice of suitable bus architecture type. They can be based for example on tree [2], ring [3] or classical bus [4] topology and each of them has its own (dis)advantages. The proposed architecture utilizes modified tree structure. This solution covers all useful features, it is very effective and resource-sparing as well as easily scalable and maintainable.

2. PROPOSED SOLUTION

The interconnection system is a generic system of high throughput internal buses dedicated both for communication between FPGA components and for their communication with other computer devices which are mapped to the host system memory. The buses are full duplex and packet-oriented so the data can be transferred simultaneously in both directions.

The data width is configurable, individually for every bus part (branch). Due to this very important feature, it is possible to build uniform hierarchical system of internal buses with different speed that interconnects differently fast components. There is no need to utilize many types of buses and communication protocols and whole interconnection system can be composed only of 3 universal generic components (Switch, Endpoint and Transformer).

2.1. ARCHITECTURE

The proposed architecture is based on the concept of switched tree topology. It enables the components to communicate with each other in separate branches without wasting the bandwidth of the bus on a higher level. As shown in figure 2, the tree architecture can be also redrawn as bus architecture with pipeline stages in the form of switch components. This kind of pipelining is very important in the FPGA context because wide buses are usually sensitive to distance due to limited FPGA wire routing resources.

The configurable data width (1-128 bits) enables to build the hierarchy of differently wide buses. As shown in figure 1, the biggest width is mostly at the root and such a bus connects fast components, the smallest width is on lower levels where slow components are placed.

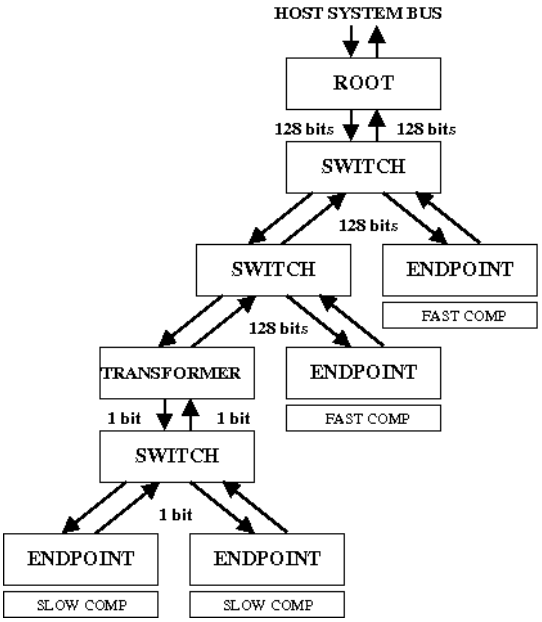

Figure 1: Tree architecture example

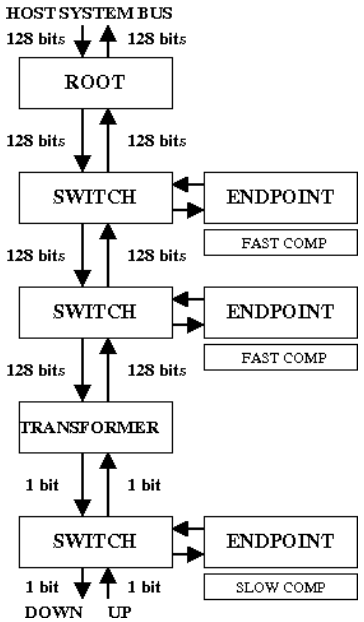

Figure 2: Tree redrawn as a bus

The highest node of a tree topology is the root. It provides the I/O interface to the host system which internal bus is connected to. This component is platform-dependant and a part of its architecture is specific for every host bus (PCI, PCI-X, PCI Express etc.). The proper independent interconnection system is composed of only 3 components – Switch, Endpoint and Transformer. The switch component performs transaction routing and

switches packets from one port to another. Transformer converts data width which is essential from the view of whole hierarchy. The most complex component is Endpoint. It provides write and read interface for connected user components. The read interface has 2 variants: packet (one-shot request handover) and continual (successive address increment). It is possible to set if strict transaction order is kept or not.

One of the essential features is also the support of transfers initiated from the side of internal components, so called bus master transfers. This feature is optional for every communication node (Switch) as well as for every point of connection (Endpoint). So two variants (slave, master) of these components are available and the right choice of one of them leads to the reduction of utilized resources.

2.2. COMMUNICATION PROTOCOL

The internal bus uses a packet-based communication protocol (figure 3 and 4). Each packet consists of a header and optionally data payload. The header carries necessary control information. The packets are marked by Start-Of-Packet (SOF_N) and End-Of-Packet (EOF_N) signals. Packet data transfer is controlled by means of Source Ready (SRC_RDY_N) and Destination Ready (DST_RDY_N) signals. Using these two signals, the communication can be easily stopped by either the receiver or the transmitter.

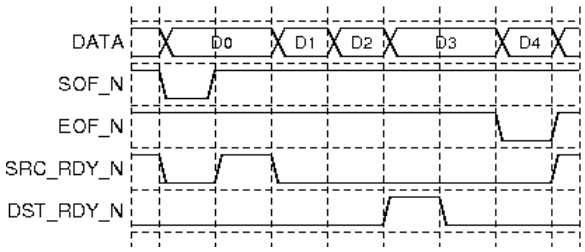

Figure 3: Communication protocol

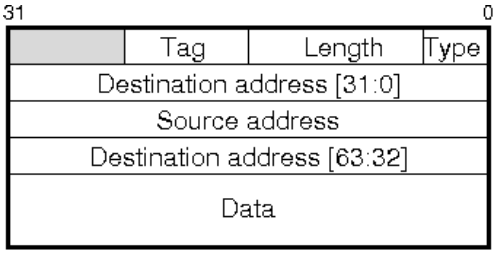

Figure 4: Packet format

3. CONCLUSION

This paper introduced generic interconnection bus system. Due to well designed architecture based on tree topology and configurable data width, it is possible to build uniform hierarchical system of full duplex, packet-orientated internal buses with different speed that interconnects differently fast components. The proposed architecture is despite high throughput universal, resource-sparing, well scalable and easily maintainable. The system is intended for chips with FPGA technology but due to separating of platform-dependant and independent parts, it is also portable into other technologies.

REFERENCES

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